"An ATM Cell Processor"

INTRODUCTION

Field of the Invention

The invention relates to a processor for handling asynchronous transfer mode (ATM) cells.

Prior Art Discussion

The ATM technique supports many different services such as voice, frame relay, or circuit emulation. Also, the throughput rates are quite high, in the order of hundreds of thousands of cells per second.

The general approach has been to provide extensive circuitry to handle the many cell processing functions required. For example, European Patent Specification No. EP614324 (Nippon) describes circuitry having cell assembly and disassembly control circuits and memory access control circuits.

Such circuits tend to be limited in their functionality and to be complex.

Objects of the Invention

An object of the invention is to provide for efficient handling of cells by a processor. Another object is that the processor has flexibility in the manner in which it operates so that it may be used in different environments with relatively simple configuration.

A still further object is to provide a cell processor which may be controlled in a comprehensive manner with relatively simple control circuits.

SUMMARY OF THE INVENTION

According to the invention, there is provided an ATM cell processor comprising a line interface, a backplane interface, and processing means for identifying cells according to their headers and processing the identified cells.

Thus the processor may be integrated in a flexible manner in a system having multiple cell streams.

In one embodiment, the line and backplane interfaces are bi-directional. This provides excellent versatility for cell processing.

In one embodiment, the processing means comprises a mapping function. This allows mapping of received cells according to the VPI/VCI.

Preferably, the mapping function comprises means for changing the cell headers according to mapped cell destinations.

In one embodiment, the mapping function comprises means for adding an additional header to a cell for internal control signalling.

In another embodiment, the processing means further comprises a policing function for monitoring traffic characteristics. This allows integration in a system connected to multiple client systems and is particularly useful for monitoring contracts.

In a further embodiment, the processing means comprises a queueing function connected between the interfaces for controlling transfer of cells to the line interface. This provides for effective cell traffic management.

In another embodiment, the queueing function comprises means for interfacing with a cell memory for storage of cell queues, and with a control memory for storing queueing

parameter values. This enhances flexibility in the manner in which cells are queued. It also provides for simple queueing control.

In one embodiment, the queueing function is connected to a memory controller for interfacing with the cell and control memories.

Preferably, the queueing function comprises means for managing path descriptor tables in the control memory.

In another embodiment, the queueing function comprises means for managing queue descriptor tables, each relating to individual queues in the control memory.

In one embodiment, the cell processor further comprises a segmentation and reassembly (SAR) interface for routing of cells to an external SAR device. This allows connection of the cell processor to a control processor in an efficient manner using cells for control signalling.

Preferably, the SAR interface is connected to the queueing function.

In one embodiment, the cell processor comprises a control processor interface for connection to a memory controller to allow initial set-up configuration.

DETAILED DESCRIPTION OF THE INVENTION

Brief Description of the Drawings

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a schematic representation of a cell processor of the invention;

Fig. 2 is a diagram illustrating operation of a queue server matrix; and

Fig. 3 is a diagram illustrating a UTOPIA interface of the cell processor.

Description of Embodiments

Referring to Fig. 1, there is shown a cell processor 10 of the invention. The processor 10 is an application specific integrated circuit (ASIC), the application being processing of ATM cells.

The main components of the ASIC 10 are now briefly described briefly with reference to general signal flows through the processor. The cell rate handled is 373 K cells per second, which represents a bit rate of greater than 155 Mpps. The ASIC 10 has a backplane interface 11 for interfacing according to the CUBIT™ protocol via a backplane.

A queueing function 12 performs extensive buffering operations using DRAM or SRAM external to the ASIC 10 and is accessed via a CellRAM controller 13. It also uses an SRAM controller 14 for access to additional off-chip SRAM. The off-chip memory is used in general for such things as manipulating link lists, and storing cells awaiting transfer. More specifically, the SRAM accessed by the SRAM controller 14 is used effectively as an external register and to store queue parameters including the queue sizes. On the other hand, the DRAM or SRAM accessed via the CellRAM controller 13 is used for storing actual cells. When dequeueing from the Cell RAM, the SRAM is used to track the cells using pointer information.

Cells received in the direction A at the backplane interface 11 are passed to the queueing function 12, and may be routed to CellRAM. Continuing on the path A indicated in Fig. 1, the cells are then transferred to a multi-PHY line interface 15. This is a master

interface which supports many ports, in this embodiment eight. Again, the UTOPIA protocol is used.

Thus, in the path A, the ASIC 10 does not change the cells, but does manage output to the line by using queueing mechanisms and external memory.

In the opposite direction, cells are received as indicated by the arrow B at the line interface 15 and are transferred to a mapping function 16. The mapping function 16 changes the VCI/VPI headers according to the destination of the cells and by doing this, it re-directs them to the correct destination. It does not "know" what the different cell streams represent, but it identifies the streams by their headers. The cells are passed to a policing function 17 which operates according to algorithms to evaluate certain policing parameters such as the cell rate for a particular contract. Various parameters are taken into account such as the temporary nature of any usage of excessive bandwidth for a particular contract. The SRAM accessed via the SRAM controller 14 is used for some of these functions. After the policing functions, the cells are transferred to the backplane interface 11.

The ASIC 10 also comprises a processor interface 20 and a configuration and status function 21, which are connected to the queueing function 12 and the SRAM controller 14. This allows a microprocessor to access the ASIC 10 and perform a limited set of functions including initial setup and configuration and subsequent status monitoring. An important initial setup function is configuration of the SRAM 14. Subsequently, the processor can access the SRAM locations via the controller 14 and the interface 20 to monitor parameters such as the count of dropped cells.

An important aspect of the ASIC 10 is that it can use control signals communicated in the ATM format. To do this, it uses a segmentation and reassembly (SAR) interface 25 which is connected to a SAR device which performs AAL5 segmentation and reassembly of ATM messages. This interface is used for communication of ATM messages with a SAR device. The SAR device interfaces with another device such as a microprocessor

(possibly the same microprocessor as is connected to the interface 20) for comprehensive control communication. The ATM nature of the communication is transparent to the microprocessor because of operation of the SAR device. Thus, a single microprocessor may have access to the ASIC 10 in two different manners, one being a direct access for initial setup and monitoring of parameters, the other being for comprehensive control communication.

Referring again to the direction A of Fig. 1 the cells which are received at the backplane interface 11 are queued in one of the multiple queues depending on their VPI/VCI. The queues are serviced on a pre-programmed basis to implement a priority queueing system. Queues that grow too large may have cells discarded on a configured basis. Statistics are kept on the number of cells received, the number of cells transmitted, the number of bad cells, and the number of cells dropped due to congestion.

Queueing is initialised by a microprocessor using the configuration and status function 21. This function has registers, in which there is a notional split of registers related to queueing and those related to dequeueing. The queueing function 12 uses a significant number of tables to control the buffering and congestion management functions. One such table is a path descriptor, the start address of which is provided by a configuration register. The VPI of an incoming cell is used to form an offset into this table. In addition there are special path descriptors for mapping, for the SAR, and for the processor, the addresses again being provided by configuration registers.

Another table is a queue descriptor, which contains information about an individual queue. All queues are identical, however, they may appear to have different priorities depending on programming of a queue server matrix. Queues are irrevocably tied to target output ports and each of the eight line ports has eight queues associated with it. In addition, a single queue is maintained for each of the processor, SAR, and mapping entities. Mapping between queues and targets is specified in two tables, one for each of aggregate and tributary modes. Each queue has a four-word descriptor, and the offset

from the value of the configuration register holding the start location is simply the queue number multiplied by four.

A queue server matrix 30 is shown in Fig. 2. It controls the order in which queues are serviced. Its location and maximum size (1024 elements) are indicated by configuration registers. Each element (31) of the matrix holds eleven used fields. Each field is associated with a queue. The queues are checked in ascending order, i.e. the first queue checked is the most significant byte of the first word. Within each byte, only the least significant seven bits are meaningful, i.e. bits 6 to 0. The value in a field indicates the priority level for the associated queue.

Storage pools of the queues are referred to as heaps, and consist of stacks of DRAM addresses. There are twenty heaps maintained. The heap structure is implemented as a set of pointers kept internally and also the DRAM addresses which are stored in the SRAM. Initialisation of the heap involves programming up the pointers into SRAM for the top-of-stack and start-of-stack for each used heap, and then initialisation of the SRAM location between those two pointer values with a unique and valid set of DRAM locations. Configuration registers are used for programming the heap pointers.

These features provide excellent flexibility in the manner in which queues are set up and dynamically managed.

As shown in Fig. 1, the output cells of the queueing function are transferred to the line interface 15 or the SAR interface 25.

In the opposite direction, cells received at the line interface 15 are passed to the mapping and policing functions 16 and 17. The cells are passed to the backplane interface 11, to the queueing function 12, or are dropped. Again, the configuration registers store the initialisation information. SRAM tables are maintained by the functions 16 and 17. There are five tables associated with the mapping function 16 as follows:

- per port statistics table,
- VCC connection table,
- dequeue connection table, and
- secondary mapping descriptor table.

Storage of these tables is set by the configuration registers. The per port statistics table stores information including the numbers of cells with invalid and disabled VPI/VCIs and with unsupported PTIs. It also includes the VPI/VCIs of the last disabled and invalid cells.

The VCC connection table contains the following information on a per connection basis:-

mapping descriptor,

received cell count,

dropped cell count, and

GCRA words 1 – 4.

The VPC connection table is identical, except that VPIs are used in place of VCIs.

The dequeue connection table has a maximum of 1024 entries and consists of 1024 32 bit mapping descriptors.

The secondary mapping descriptor table consists of 4096 32 bit entries. Each secondary mapping descriptor is 14 bits long, as set out below.

Field Name	Size	Bit Position
Reserved	18	14-31
map_vpi	1	13
cell_routing	3	10-12
vci_map	10	0-9

Referring now to the three UTOPIA interfaces 11, 15, and 25, Fig. 3 shows an overview. All of the interfaces use the appropriate Start-of-Cell (SOC) signal to initialise cell reception from an external source. Each interface counts octets and an error indication is given when a SOC is activated at an unexpected time. This gives a warning of malformed cells entering the ASIC whilst providing a mechanism to recover at the next cell boundary. Short cells are discarded, whilst long cells are truncated and passed on. Both cause an error indication. Before cells are transferred internally, they are synchronised to the internal common system clock "sys clk". A phase locked loop (PLL) 40 provides the internal clock signal from an external microprocessor 42. A SAR device 43 is shown connected to the SAR interface 25. Also, line and backplane devices 44 and 45 are shown connected to their respective interfaces.

It will be appreciated that the invention provides for very efficient processing of ATM cells between a line and a backplane. Varying rates of cell transfer are handled effectively by the queueing mechanism. The circuit also supports many different services by efficiently routing cell streams. The circuit also allows policing functions to be implemented very efficiently with little effect on cell transfer rates.

The invention is not limited to the embodiments described, but may be varied in construction and detail within the scope of the claims.